IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
COFFA ET AL.

Serial No. **NOT YET ASSIGNED**

Filing Date: **HEREWITH**

For: **PRESSURE SENSOR MONOLITHICALLY INTEGRATED AND RELATIVE PROCESS OF FABRICATION**

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DATE OF DEPOSIT DEC. 11, 2001

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DAWN KIMLER
(TYPED OR PRINTED NAME OF PERSON MAILING PAPER OR FEE)

Dawn Kimler
(SIGNATURE OF PERSON MAILING PAPER OR FEE)

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for a proposed drawing modification as indicated in red ink to label FIGS 1 and 2a to 2d as prior art. FIGS. 1- 3h are also being modified to delete certain extraneous markings and add reference numerals. No new matter is being entered.

In the Claims:

Please cancel Claims 1 to 8.

Please add new Claims 9 to 47.

9. A process of fabricating a pressure sensor comprising:

forming a buried layer of second conductivity type in a substrate of first conductivity type and forming an upper layer of first conductivity type adjacent the buried layer;

forming at least one opening to a depth sufficient to reach the buried layer;

selectively etching the buried layer through the at least one opening to make the buried layer porous;

forming a sacrificial layer on the upper layer;

forming a backplate over the sacrificial layer; and

removing the sacrificial layer and porous buried layer to thereby define a cavity and adjacent diaphragm for the pressure sensor.

10. A process according to Claim 9 further comprising forming a plurality of holes in the backplate.

11. A process according to Claim 9 wherein the cavity and adjacent diaphragm are shaped as concentric circular sectors.

12. A process according to Claim 9 further comprising forming a sealant layer for the at least one opening prior to forming the sacrificial layer; and etching the sealant layer to reopen the at least one opening before the removing.

13. A process according to Claim 12 wherein the sealant layer and the sacrificial layer both comprise silicon oxide deposited by a PVAPOX technique.

14. A process according to Claim 9 wherein the removing comprises oxidizing the porous buried layer and etching the oxidized porous buried layer.

15. A process according to Claim 14 wherein the oxidizing is carried out immediately after selectively etching the buried layer.

16. A process according to Claim 14 wherein the etching comprises isotropically etching with an acid solution.

17. A process according to Claim 16 wherein the acid solution comprises a diluted solution of hydrofluoric acid and the etching is carried out at room temperature.

18. A process according to Claim 9 wherein the substrate comprises monocrystalline silicon; and wherein forming the backplate comprises forming the backplate comprising polycrystalline silicon.

19. A process according to Claim 9 wherein selectively etching the buried layer comprises electrochemically etching the buried layer using an electrolytic solution.

20. A process according to Claim 9 wherein forming the at least one opening comprises forming a plurality of openings equally spaced apart.

21. A process according to Claim 9 wherein forming the at least one opening comprises forming the at least one opening by masking and anisotropic plasma etching.

22. A process according to Claim 9 wherein forming the at least one opening comprises forming the at least one opening through a face of the substrate opposite the upper layer.

23. A process according to Claim 9 wherein forming the at least one opening comprises forming the at least one opening through a face of the upper layer opposite the substrate.

24. A process according to Claim 9 wherein the substrate comprises monocrystalline silicon and the upper layer comprises an epitaxial silicon layer.

25. A process of fabricating a pressure sensor comprising:

forming a buried layer of second conductivity type between first and second layers of first conductivity type;

forming at least one opening to a depth sufficient to reach the buried layer;

selectively treating the buried layer through the at least one opening;

forming a sealant layer for the at least one opening;

forming a sacrificial layer adjacent the upper layer and sealant layer;

forming a backplate over the sacrificial layer with a plurality of holes therein;

etching the sealant layer to reopen the at least one opening; and

removing the sacrificial layer and the treated buried layer to thereby define a cavity and adjacent diaphragm for the pressure sensor.

26. A process according to Claim 25 wherein the cavity and adjacent diaphragm are shaped as concentric circular sectors.

27. A process according to Claim 25 wherein removing comprises oxidizing the treated buried layer and etching the oxidized treated buried layer.

28. A process according to Claim 27 wherein the oxidizing is carried out immediately after selectively treating the buried layer.

29. A process according to Claim 27 wherein the etching comprises isotropically etching with an acid solution carried out at room temperature.

30. A process according to Claim 25 wherein the substrate comprises monocrystalline silicon; and wherein forming the backplate comprises forming the backplate comprising polycrystalline silicon.

31. A process according to Claim 25 wherein selectively treating the buried layer comprises electrochemically etching the buried layer using an electrolytic solution.

32. A process according to Claim 25 wherein the first layer comprises a substrate and the second layer comprises an epitaxial layer formed thereon; and wherein forming the at least one opening comprises forming the at least one opening through the epitaxial layer.

33. A monolithic pressure sensor comprising:

a substrate having a first conductivity type;

a buried layer of a second conductivity type in said substrate, said buried layer having a cavity therein for the monolithic pressure sensor;

an upper layer of first conductivity type adjacent said buried layer defining a diaphragm for the monolithic pressure sensor; and

a backplate spaced from said upper layer.

34. A monolithic pressure sensor according to Claim 33 wherein said backplate comprises a first polycrystalline silicon layer of first conductivity type and a second layer of

undoped polycrystalline silicon adjacent said first polycrystalline silicon layer.

35. A monolithic pressure sensor according to Claim 33 wherein said upper layer has a plurality of openings therein in fluid communication with the cavity.

36. A monolithic pressure sensor according to Claim 33 wherein said backplate has a plurality of openings therein.

37. A monolithic pressure sensor according to Claim 33 wherein the cavity and adjacent diaphragm are shaped as concentric circular sectors.

38. A monolithic pressure sensor according to Claim 33 wherein said substrate comprises monocrystalline silicon; and wherein said backplate comprises polycrystalline silicon.

39. A monolithic pressure sensor according to Claim 33 wherein said substrate comprises monocrystalline silicon; and wherein said upper layer comprises an epitaxial silicon layer on said substrate.

40. An integrated circuit comprising:

a substrate having a first conductivity type and a plurality of pressure sensors integrated thereon;

each pressure sensor comprising a buried layer of a second conductivity type in said substrate and having a cavity therein, an upper layer of first conductivity type adjacent

said buried layer and defining a diaphragm, and a backplate spaced from said upper layer; and

electronic circuitry formed in said substrate and connected to said pressure sensors.

41. An integrated circuit according to Claim 40 wherein said backplate comprises a first polycrystalline silicon layer of first conductivity type and a second layer of undoped polycrystalline silicon adjacent said first polycrystalline silicon layer.

42. An integrated circuit according to Claim 40 wherein said upper layer has a plurality of openings therein in third communication with the cavity.

43. An integrated circuit according to Claim 40 wherein said backplate has a plurality of openings therein.

44. An integrated circuit according to Claim 40 wherein the cavity and adjacent diaphragm are shaped as concentric circular sectors.

45. An integrated circuit according to Claim 40 wherein said substrate comprises monocrystalline silicon; and wherein said backplate comprises polycrystalline silicon.

46. An integrated circuit according to Claim 40 wherein said substrate comprises monocrystalline silicon; and

wherein said upper layer comprises an epitaxial silicon layer on said substrate.

47. An integrated circuit according to Claim 40 wherein said electronic circuitry comprises:

a respective analog/digital converter for each pressure sensor; and

a processor connected to said analog/digital converters for performing a time-delay correlation between signals produced by different pressure sensors and generating a value of delay for which the time-delay correlation is maximum, and for calculating a direction of a sound source for a sound wave as sensed by said pressure sensors based upon the time delays.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is

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encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

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[signature]
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SUBMISSION OF PROPOSED MODIFICATIONS TO DRAWINGS

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Submitted herewith is a request for a proposed drawing modification as indicated in red ink to label FIGS 1 and 2a to 2d as prior art. FIGS. 1- 3h are also being modified to delete certain extraneous markings and add reference numerals. No new matter is being entered.

Respectfully submitted,

[signature]

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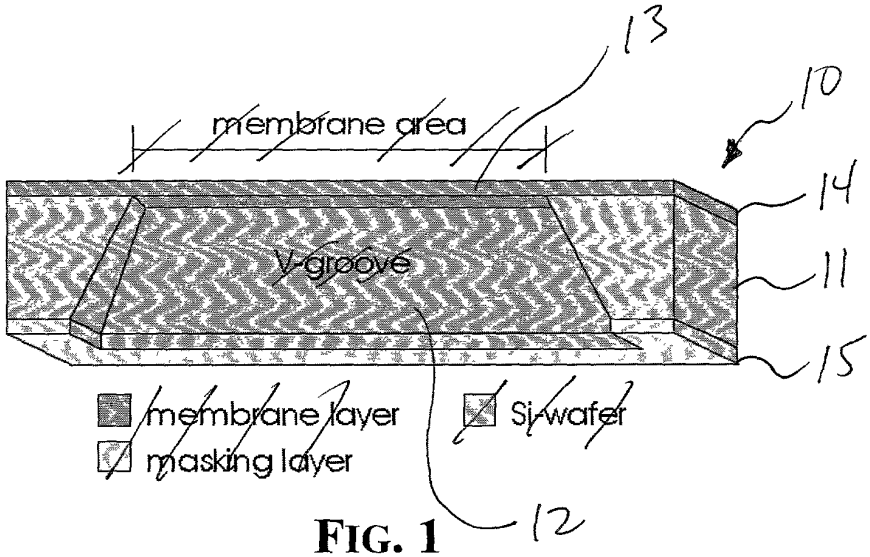


FIG. 1
PRIOR ART

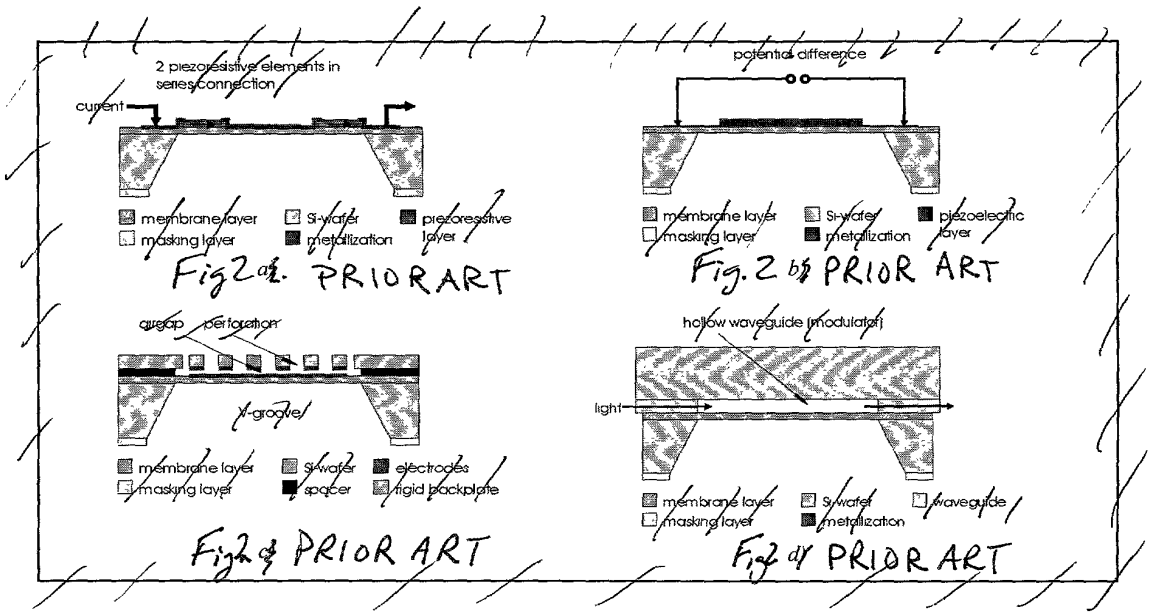
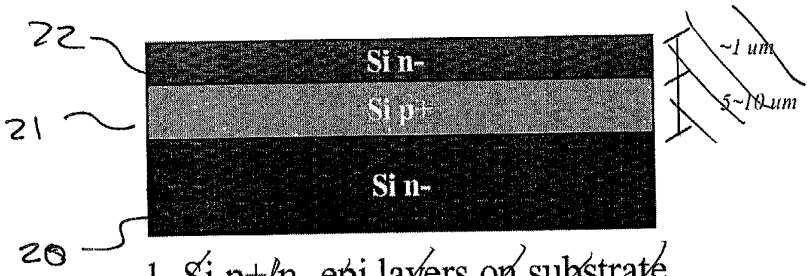
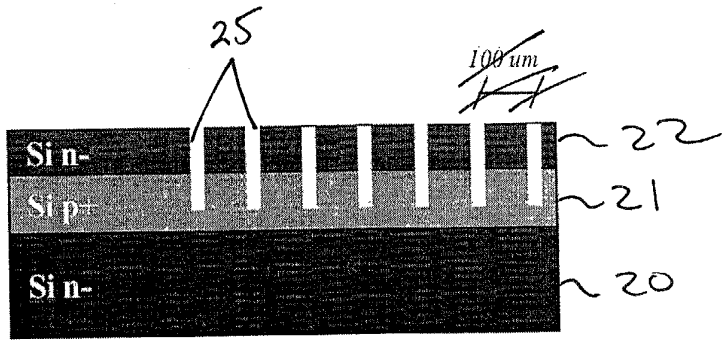


FIG. 2



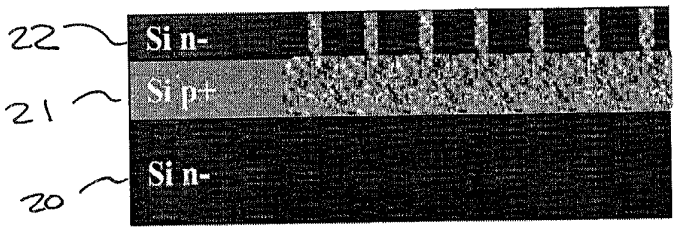
1. Si p+/n- epi layers on substrate

FIG. 3A



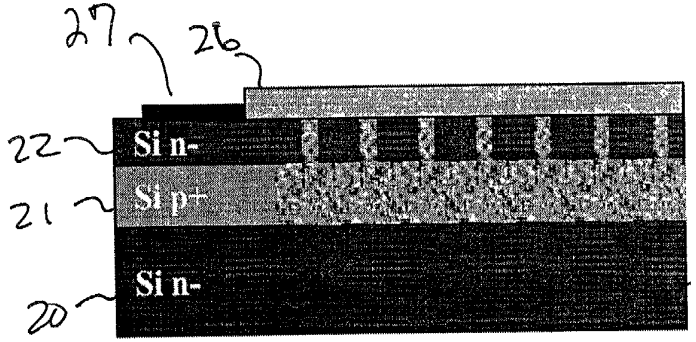
2. Trench formation by plasma etching (and mask opening)

FIG. 3B



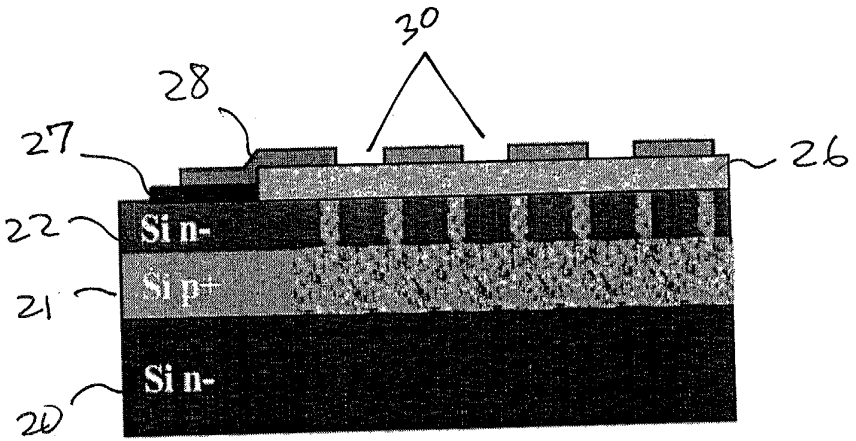
3. Si Porous formation in p+ by electrochemical attack
4. Trench filling and surface planarization

FIG. 3C



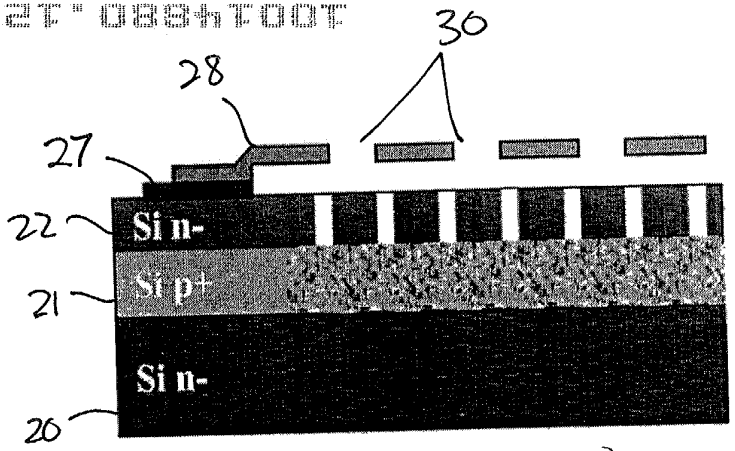
5. Deposition and patterning of the sacrificial layer
6. Nitride isolation layer

FIG. 3D



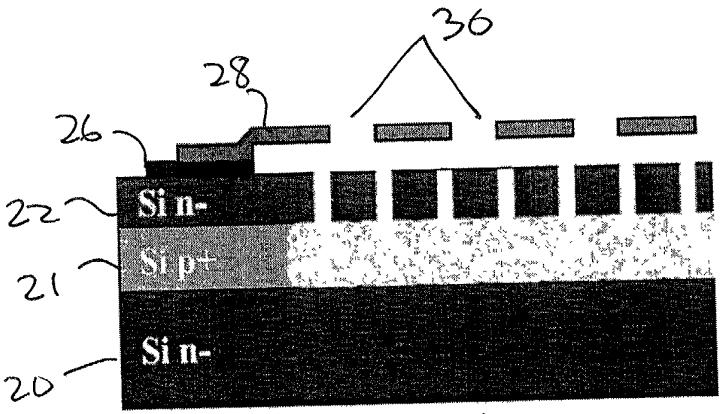
7. PoliSi n+ formation for backplate

FIG. 3E e



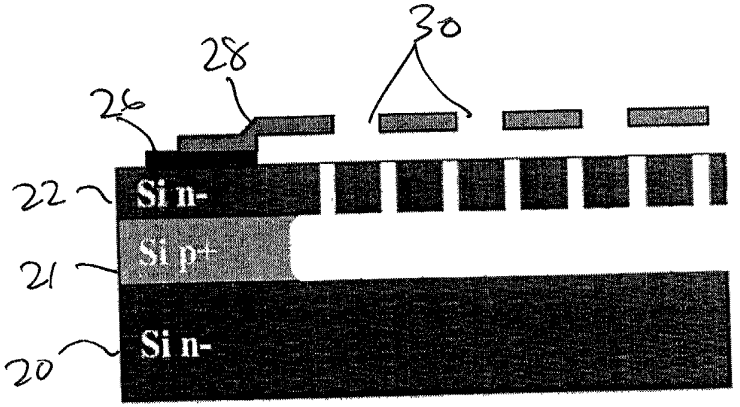
8. Removal of the sacrificial layer (HF attack)

FIG. 3F f



9. Si-porous Oxidation

FIG. 3G g



10. Removal of Si-porous

FIG. 3H h

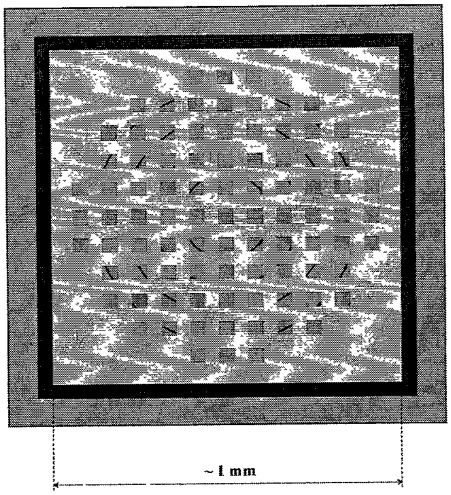

~1 mm

FIG. 4

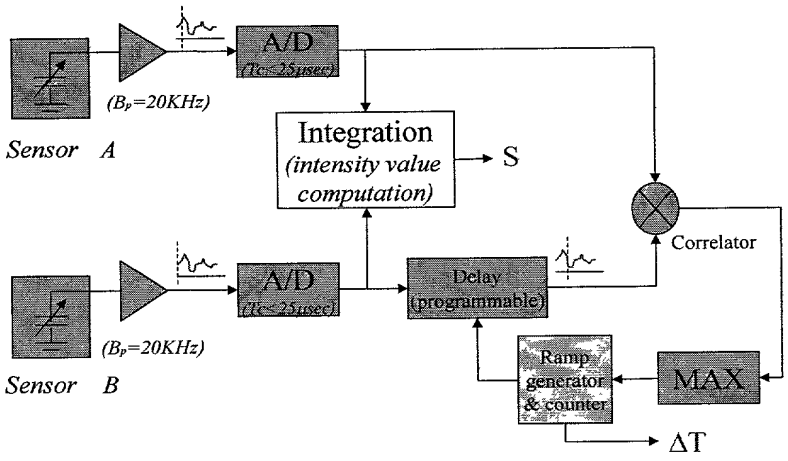

A/D
(Tc=25μsec)
(Bp=20KHz)
Sensor A
Integration
(intensity value computation)
S
Correlator
A/D
(Tc=25μsec)
Delay
(programmable)
(Bp=20KHz)
Sensor B
Ramp generator & counter
MAX
ΔT

FIG. 5